



Power Design Manager (PDM) 2022.2 for XRTC

Jim Devereaux
FAE Los Angeles Area
Nov 23, 2022

Agenda

- Why change XPE
- Introducing Power Design Manager 2022.2
- PDM roadmap
- Available Resources
- Demo

Why change XPE?

XPE Has served us well, why change?

XPE Is

- Critical Pre-Design tool
- Scope has grown over 15+ years to cover:
- Thermal Specification tool
- Necessary for board designs
- Datasheet for Xilinx Power

1. XPE launched in 2006 supporting Virtex-4... a lot has changed
2. Device complexity | Perf/W has increased significantly in that time
3. SoC, RFSoc, AI Engines, NoC, Hard IPs....
4. System Level capability needed

XPE IS NOT

- A Viable future platform
 - MS Excel going to the cloud
- Agile enough to meet our requirements
- Able to handle extra device complexity
- A Scalable tool

Adapt to Changing User Base & Strategy:



XPE Designed for
Traditional FPGA
Designers



XPE only supports
Chip-level Design



Next Generation ACAP
Designers



SOM



System Architects



Alveo



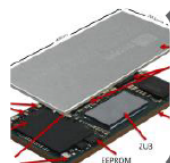
PCB Designers



Evaluation Boards



Software/Algorithm
Developers



3rd Party & Customer Boards /
SIPs

Introducing Power Design Manager 2022.2

Power Design Manager (PDM) *Next Generation Power Estimation Tool*

- Leverages Vivado infrastructure
 - Stand alone download, no dependencies on Vivado
 - Integration to unified installer 2023.1
 - No License required for general access devices
- Initial Release coming in 2022.2
 - Support for all Versal® public devices
 - Versal® : AI Core | Prime | Premium | AI Edge
 - Kria™ : K26 & KV260
- 2022.2 will focus on
 - EoU, Tool Stability
 - Enhanced wizard for hardened blocks
 - Clocking | DDRMC | MRMAC | DCMAC | ILKN | HSC | CPM/5 | PCIe
 - Generation of XDC constraints and XML file
 - Simple Migration from XPE
 - Support for Windows and Linux
- All new device support will be PDM only
 - Versal® HBM coming 2023.1

The screenshot displays the Power Design Manager (PDM) interface within a Vivado environment. The main window shows a 'Summary' tab with various configuration options and power estimation results.

Configuration:

- Family: Versal AI Edge Series
- Device Grade: XC
- Device: XCVE2802
- Package: NSVH1369
- Speed: 1
- Static Power: Low
- Temperature: Industrial -40C->100C
- VCCINT Voltage: Low - 0.70v, PS at 0.88v
- Process: Typical

Vivado part: XCVE2802-NSVH1369-1LHP-LL

Summary:

Summary	Value
Total On-Chip Power (W)	4.079 W
Junction Temperature (Tj)	25 C
Thermal Margin	75 C
Thermal Power Margin	0.000 W
Characterization	Advance (+/- 25% accuracy)

Environment:

Environment	Value
Junction Temperature (C)	25 C
Ambient Temperature (Ta)	25 C
Effective ThetaJA	0.000 C/W
Max. Junction Temperature	100 C
Design Power Budget	

On-Chip Power:

Resource	Power (W)	Power (%)
PMC	0.248 W	6.09 %
Processing System		
LPD	0.000 W	0.00 %
FPD	0.000 W	0.00 %
Network On Chip	0.166 W	4.08 %
Programmable Logic		
Clocking	0.343 W	8.41 %
Logic	0.810 W	19.86 %
BRAM	0.001 W	0.02 %
URAM	0.000 W	0.00 %
DSP	0.000 W	0.00 %
MMCM	0.000 W	0.00 %

Project Summary:

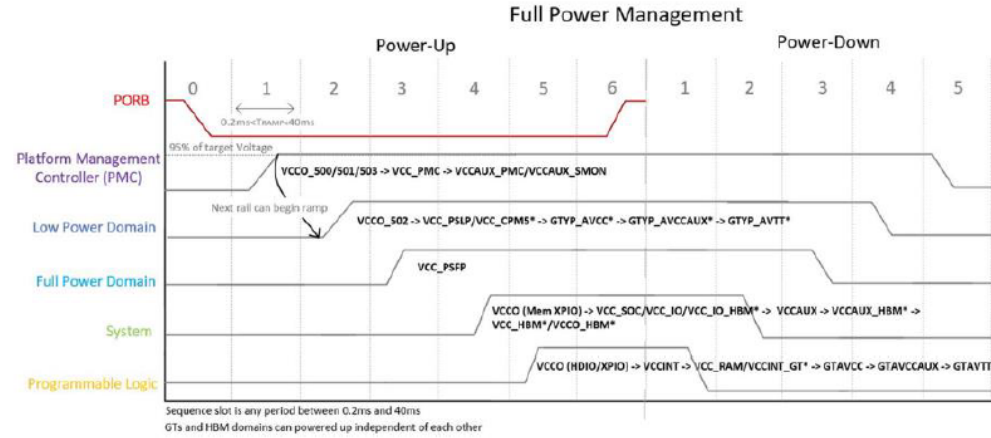
Power	Value	Percentage
Total	4.079 W	
XCVE2802-NSVH1369-1LHP-LL	4.079 W	99.99 %
Active	2.764 W	67.76 %
Static	1.315 W	32.23 %

Thermal:

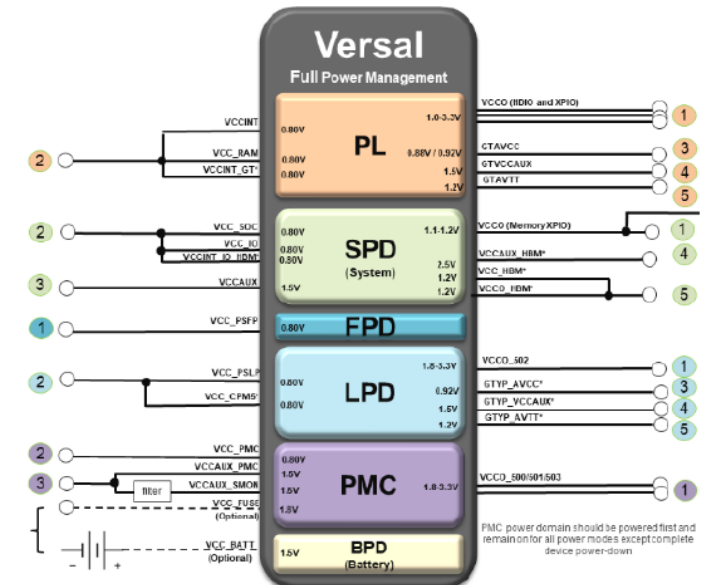
Thermal	Value
Junction Temperature (Tj)	25 C
Ambient Temperature (Ta)	25 C
Effective ThetaJA	0 C/W
Thermal Margin	75 C
Thermal Power Margin	0.000 W

Power Design Tab

- Builds on the Versal® XPE additional
- EoU and stability greatly improved
- Power on and off sequencing has been added for all variants
 - Minimum Rails and Full Power Management options
 - Core voltages - Low, Low wOD, Mid, Mid wOD, High
 - 2LI added in PDM 2022.2
- Ability to differentiate between XC | XQ | XA
 - Coming 2022.2.1



Power Rail Group	Schematic Name	Power Domain/Sequence	Voltage	AC Ripple*	DC*	Dynamic	Step Current	Total	Power Delivery Supply Current	Power Delivery Margin	330uF-1210	100uF-0805	47uF-0603	22uF-0603	10uF-0402	1.0uF-0201
1V8_PMC_IO (Digital)		PMC/1	1.800 V	4%	1%	0.004 A	0.004 A	0.004 A					1		1	
0V80_PMC (Digital)		PMC/2	0.800 V	±-17mV	1%	0.145 A	0.048 A	0.150 A					1		1	
1V5 (Digital)		PMC/3	1.500 V	2%	1%	0.064 A	0.064 A	0.068 A					1		1	
0V80_SOC_IO (Digital)		SYSTEM/2	0.800 V	±-17mV	1%	0.000 A	0.000 A	0.124 A			1	1	1		1	
1V5_VCCAUX (Digital)		SYSTEM/3	1.500 V	2%	1%	0.036 A	0.012 A	1.098 A					1		1	
1V8_PSLP_IO (Digital)		LPD/1	1.800 V	4%	1%	0.000 A	0.000 A	0.000 A					1		1	
0V80_PSLP (Digital)		LPD/2	0.800 V	±-17mV	1%	0.000 A	0.000 A	0.006 A					1		1	
0V80_P3FP (Digital)		FPD/1	0.800 V	±-17mV	1%	0.000 A	0.000 A	0.010 A					1		1	
0V80_VCCINT_RAM (Digital)		PL2	0.800 V	±-17mV	1%	1.593 A	0.398 A	2.261 A			1	1	1		1	1
0V88 (Analog)		PL3	0.880 V	±-17mV	1%	0.566 A	0.410 A	0.626 A				2	1	1	1	1
1V5 (Analog)		PL4	1.500 V	10mV pk-pk	2%	0.017 A	0.012 A	0.020 A					1		1	1
1V2 (Analog)		PL5	1.200 V	10mV pk-pk	2%	1.266 A	1.266 A	1.307 A					1		1	1



Comparing XPE and PDM power estimates

- XPE & PDM utilise the same power models
- Power correlation expected to be within $\pm 3\%$ when using PRODUCTION models
 - Accounts for rounding, decimal place change between tools
- Wider deviation for devices at PREVIEW, ADVANCE or PRELIMINARY possible
 - These can have minor changes, without causing a change in the Characterisation step
- Devices that change Characterisation between XPE and PDM will also have deviation
 - Example VP1202 will move to PRODUCTION in PDM 2022.2

Versal™ Prime Series, Versal™ Prime Series, Versal™ Prime Series

Add/Manage IP		Project	
Reset To Defaults	Confidence Level	Low - Ea	
Summary			
Total On-Chip Power	26.7 W		
Junction Temperature	85 °C		
Thermal Margin	15°C	6.7W	
Characterization	Preliminary ($\pm 20\%$ accuracy)		
On-Chip			
Resource	Power		
	(W)	(%)	
PMC	0.221	1	

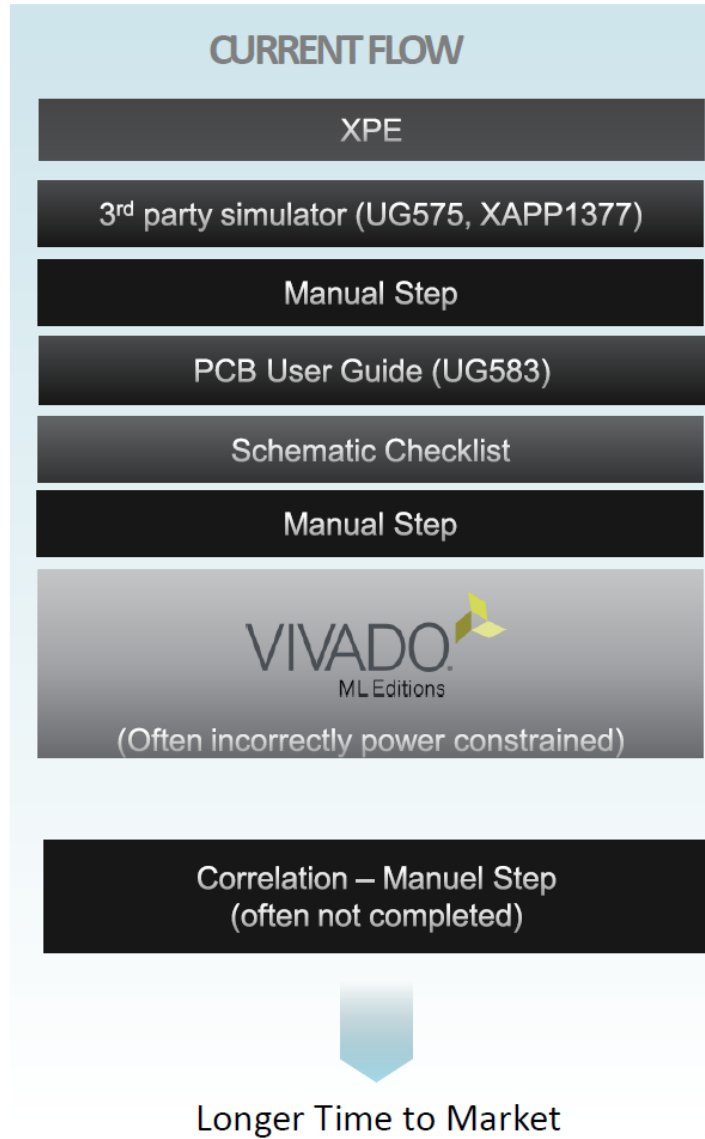
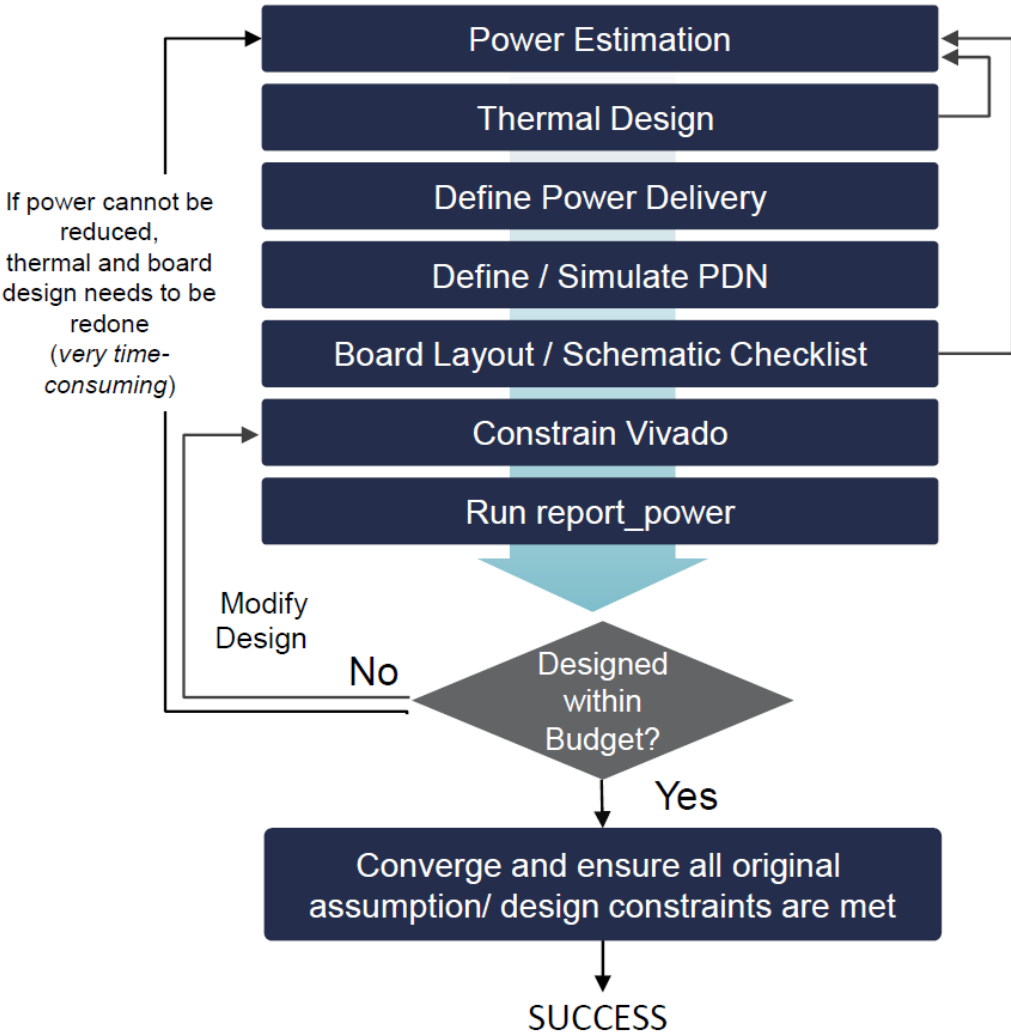
Part
Summary
Environment
DFX
On-Chip Power
Estimation
PS (0.221 W)
NoC_DDRMC (0 W)
Clock (0.94 W)
Logic (1.765 W)
Block RAM (0.259 W)
UltraRAM (1.057 W)
DSP (0.239 W)
IO (0 W)
GTYP (0 W)
GTM (7.194 W)
Hard_Blocks (1.722 W)
Power Design

Part			
Family:	Versal Premium Series	Device Grade:	XC
Device:	XCVP1202	Package:	VSVA2785
Speed:	1	Temperature:	Extended 0C->100C
Static Power:	Standard	VCCINT Voltage:	Low - 0.70v
Process:	Maximum	Vivado part: XCVP1202-VSVA2785-1LP-E-S	
Apply			
Summary		Environment	
Total On-Chip Power (W)	27.050 W	Junction Temperature (C)	User Override ON 85 C
Junction Temperature (Tj)	85 C	Ambient Temperature (Ta)	25 C
Thermal Margin	15 C	Effective ThetaJA	0.000 C/W
Thermal Power Margin		Max. Junction Temperature	100 C
Characterization	Production ($\pm 15\%$ accuracy)	Design Power Budget	

PDM Roadmap

Power Design Manager (PDM)

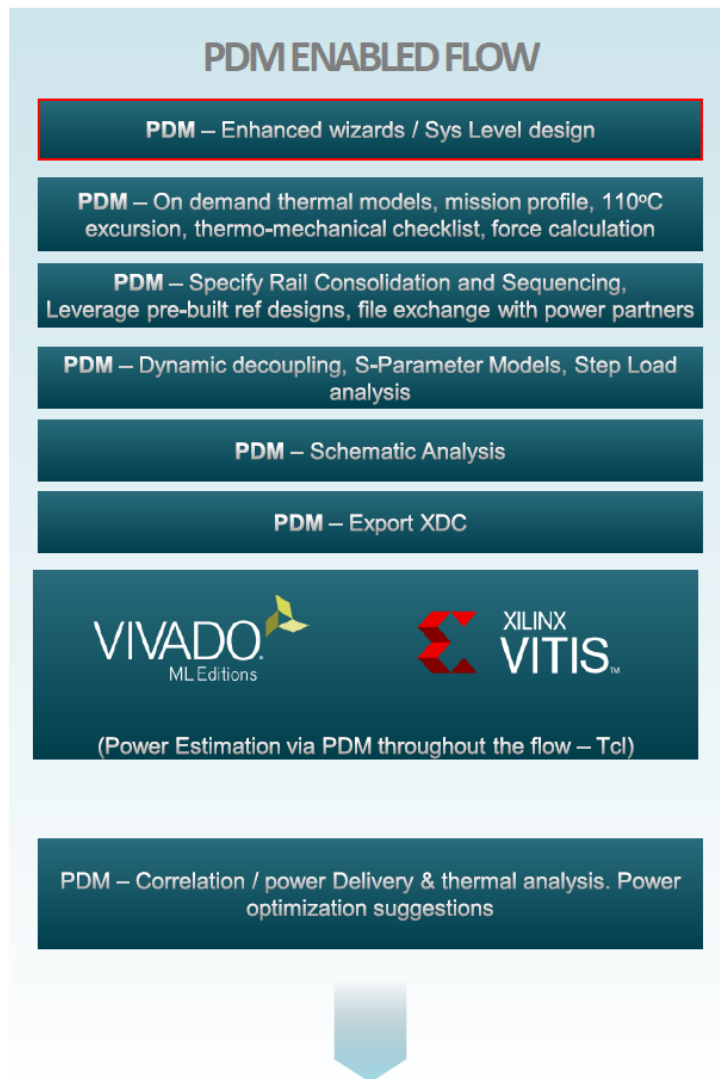
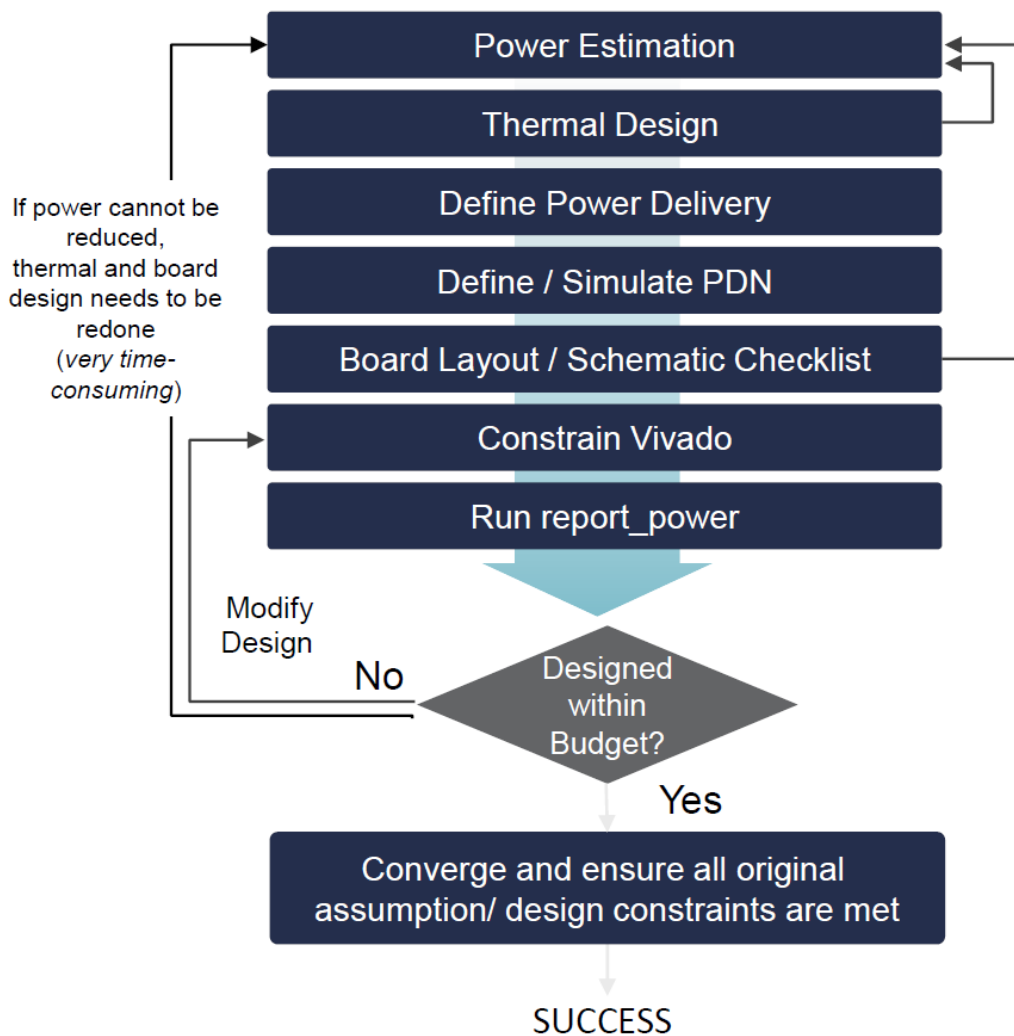
One Tool for Board Design Methodology



- Fragmented flow
 - Multiple tools and documents
- Prone to error
- Often steps missed
- Incorrect information added
- Problems are costly
 - Longer TTM & TTR

Power Design Manager (PDM)

One Tool for Board Design Methodology



Faster Time to Market

- Cohesive Managed Flow
- Aligned with Methodology
- Integrated approach
 - Addition of other tools
 - Schematic Analysis
 - SEU / FIT tool
 - Power Management
- Goals:
 - Optimal board design
 - Reduce board rework
 - Faster TTM & TTR
 - Improved customer experience
- 2022.2 focus is replacing XPE
 - Additional features 2023/24

Available Resources

- www.xilinx.com/pdm
 - Download standalone PDM install (integration to unified installer planned 2023.1)
 - No Vivado requirement for PDM
- Quick take video for PDM 2022.2 “Introduction to PDM”
 - Covers migration and Wizards
 - Getting Started and Power Design
- Customer training to be updated to PDM –ETA end Nov
- Known issues [Answer Record](#)
- Power Design Manager User Guide – [UG1556](#)

PDM Demo

Power Design Manager 2022.2 Takeaways

Increased Estimation Accuracy & Integration

- Enhanced Wizards for DDRMC | MRMAC | DCMAC | ILKN | HSC | CPM5
- Generation of XDC constraints
- Access to the latest Char models

Easy Migration from XPE

- Fast and effective migration flow from XPE for Versal® portfolio
- Re-use existing estimation
- Start new estimates for Versal® portfolio using PDM to leverage new features
- Import flow from Report Power supported

2022.2 Device and OS Support

- Windows & Linux support
- Versal® portfolio: AI Core | AI Edge | Prime | Premium
- Kria™: K26 SOM | KV260 Vision AI Starter Kit
- For more details visit www.xilinx.com/pdm

Thank you!

www.Xilinx.com/PDM