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Power Design Manager (PDM) 2022.2 for XRTC

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Agenda

- Why change XPE
- Introducing Power Design Manager 2022.2
- PDM roadmap
- Available Resources
- Demo

Why change XPE?

XPE Has served us well, why change?

XPE **Is**

- Critical Pre-Design tool
- Scope has grown over 15+ years to cover:
- Thermal Specification tool
- Necessary for board designs
- Datasheet for Xilinx Power

XPE **IS NOT**

- A Viable future platform
  - MS Excel going to the cloud
- Agile enough to meet our requirements
- Able to handle extra device complexity
- A Scalable tool

1. XPE launched in 2006 supporting Virtex-4… a lot has changed
2. Device complexity | Perf/W has increased significantly in that time
3. SoC, RFSoC, AI Engines, NoC, Hard IPs….
4. System Level capability needed

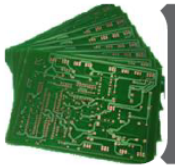
Adapt to Changing User Base & Strategy:

XPE Designed for Traditional FPGA Designers

XPE only supports Chip-level Design

Next Generation ACAP Designers

System Architects



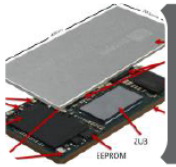
PCB Designers

Software/Algorithm Developers

SOM

Alveo

Evaluation Boards



3rd Party & Customer Boards / SIPs

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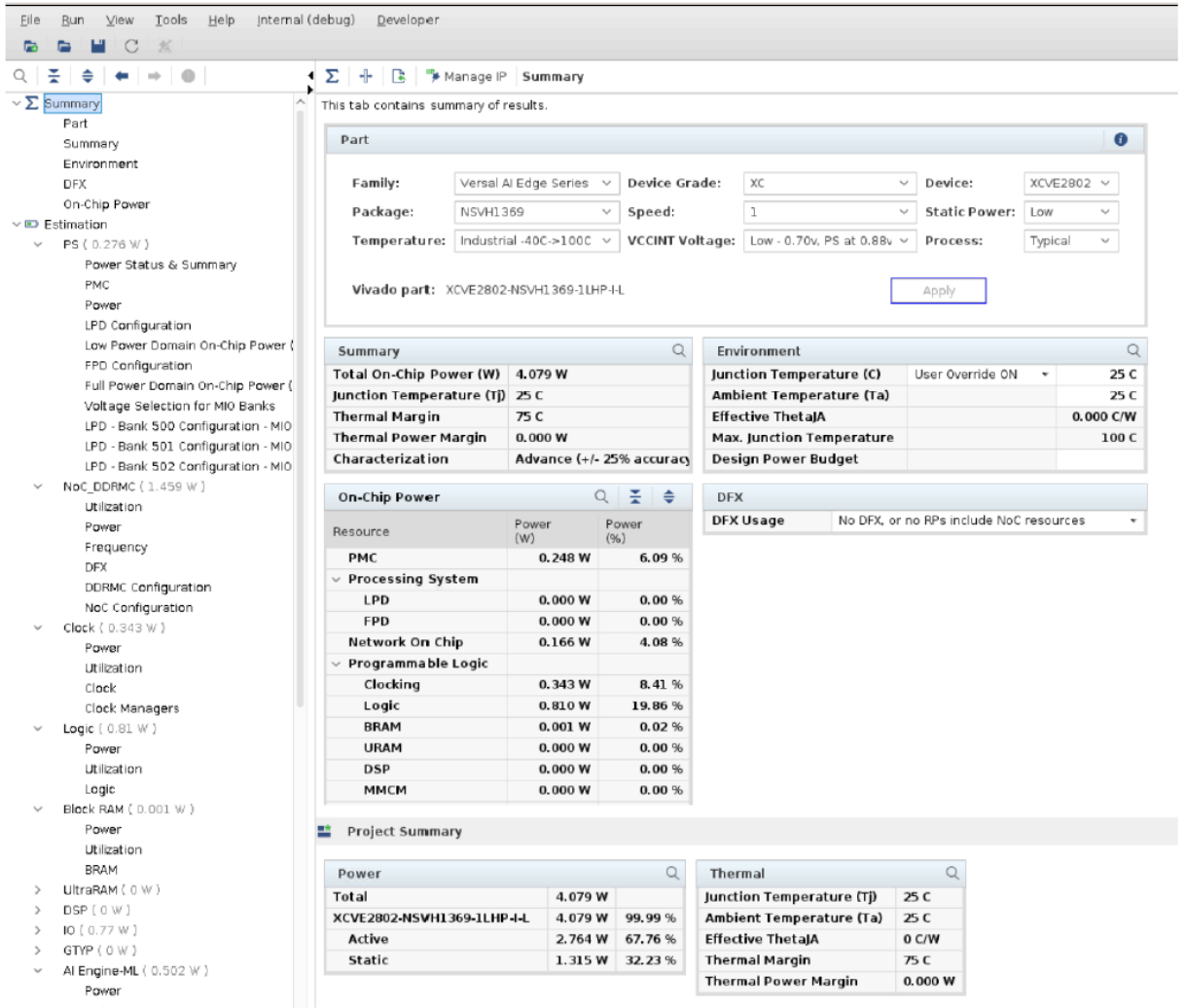
Introducing Power Design Manager 2022.2

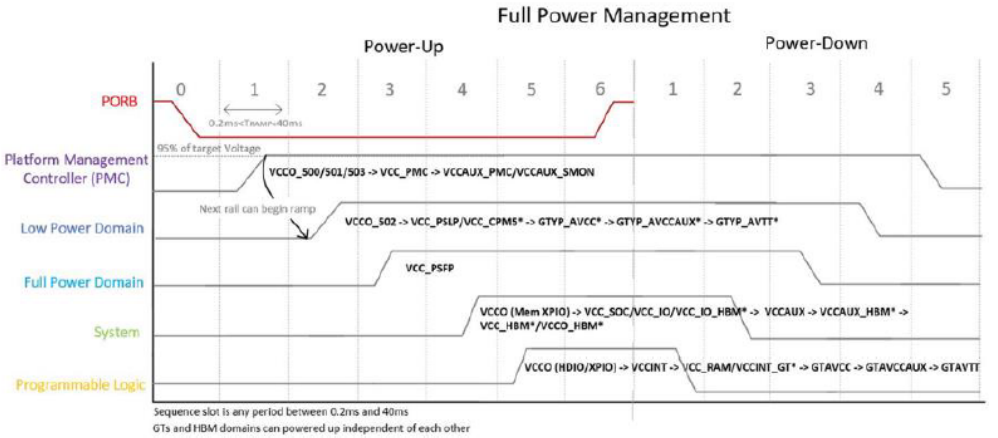
Power Design Manager (PDM) *Next Generation Power Estimation Tool*

- Leverages Vivado infrastructure
  - Stand alone download, no dependencies on Vivado
  - Integration to unified installer 2023.1
  - No License required for general access devices
- Initial Release coming in 2022.2
  - Support for all Versal® public devices
  - Versal® : AI Core | Prime | Premium | AI Edge
  - Kria™ : K26 & KV260
- 2022.2 will focus on
  - EoU, Tool Stability
  - Enhanced wizard for hardened blocks
    - Clocking | DDRMC | MRMAC | DCMAC | ILKN | HSC | CPM/5 | PCIe
    - Generation of XDC constraints and XML file
  - Simple Migration from XPE
  - Support for Windows and Linux
- All new device support will be PDM only
  - Versal® HBM coming 2023.1



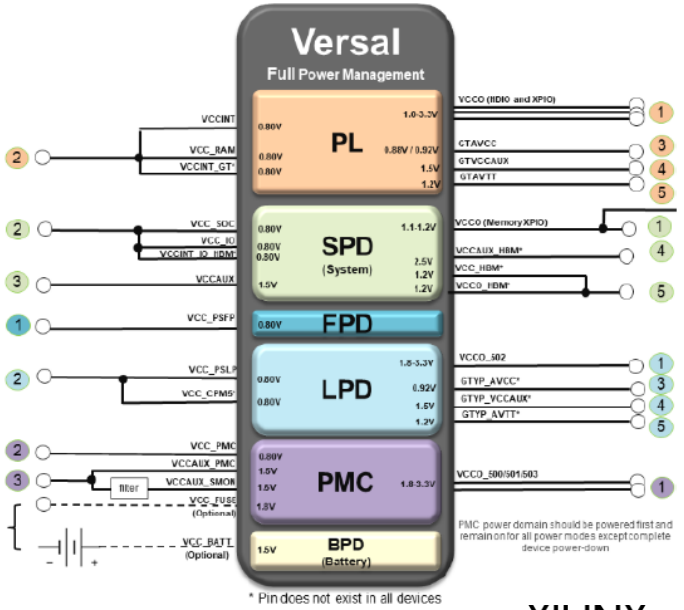
Power Design Tab

- Builds on the Versal® XPE additional
- EoU and stability greatly improved
- Power on and off sequencing has been added for all variants
  - Minimum Rails and Full Power Management options
  - Core voltages - Low, Low wOD, Mid, Mid wOD, High
  - -2LI added in PDM 2022.2
- Ability to differentiate between XC | XQ | XA
  - Coming 2022.2.1



Power Supply Design

Power Rail Group	Schematic Name	Power Domain/ Sequence	Voltage	AC Ripple*	DC*	Dynamic	Step Current	Total	Power Delivery Supply Current	Power Delivery Margin	330uF-1210	100uF-0805	47uF-0603	22uF-0603	10uF-0402	1.0uF-0201
1V8_PMC_IO (Digital)		PMC/1	1.800 V	4%	1%	0.004 A	0.004 A	0.004 A					1		1	
0V80_PMC (Digital)		PMC/2	0.800 V	+-17mV	1%	0.145 A	0.048 A	0.150 A					1		1	
1V5 (Digital)		PMC/3	1.500 V	2%	1%	0.064 A	0.064 A	0.068 A					1		1	
0V80_SOC_IO (Digital)		SYSTEM/2	0.800 V	+-17mV	1%	0.000 A	0.000 A	0.124 A			1	1	1		1	
1V5_VCCAUX (Digital)		SYSTEM/3	1.500 V	2%	1%	0.036 A	0.012 A	1.098 A					1		1	
1V8_PS_IO (Digital)		LPD/1	1.800 V	4%	1%	0.000 A	0.000 A	0.000 A					1		1	
0V80_PSLP (Digital)		LPD/2	0.800 V	+-17mV	1%	0.000 A	0.000 A	0.006 A					1		1	
0V80_PSFP (Digital)		FPD/1	0.800 V	+-17mV	1%	0.000 A	0.000 A	0.010 A					1		1	
0V80_VCCINT_RAM (Digital)		PL/2	0.800 V	+-17mV	1%	1.593 A	0.398 A	2.261 A			1	1	1		1	1
0V88 (Analog)		PL/3	0.880 V	+-17mV	1%	0.586 A	0.410 A	0.626 A				2	1	1	1	1
1V5 (Analog)		PL/4	1.500 V	10mV pk-pk	2%	0.017 A	0.012 A	0.020 A						1		1
1V2 (Analog)		PL/5	1.200 V	10mV pk-pk	2%	1.266 A	1.266 A	1.307 A					1	1	1	1



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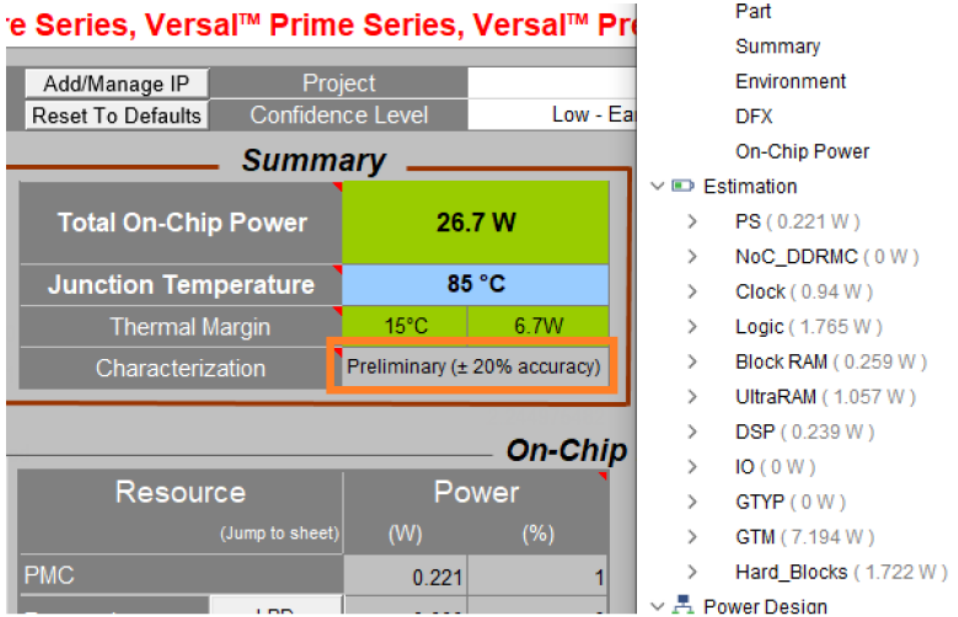
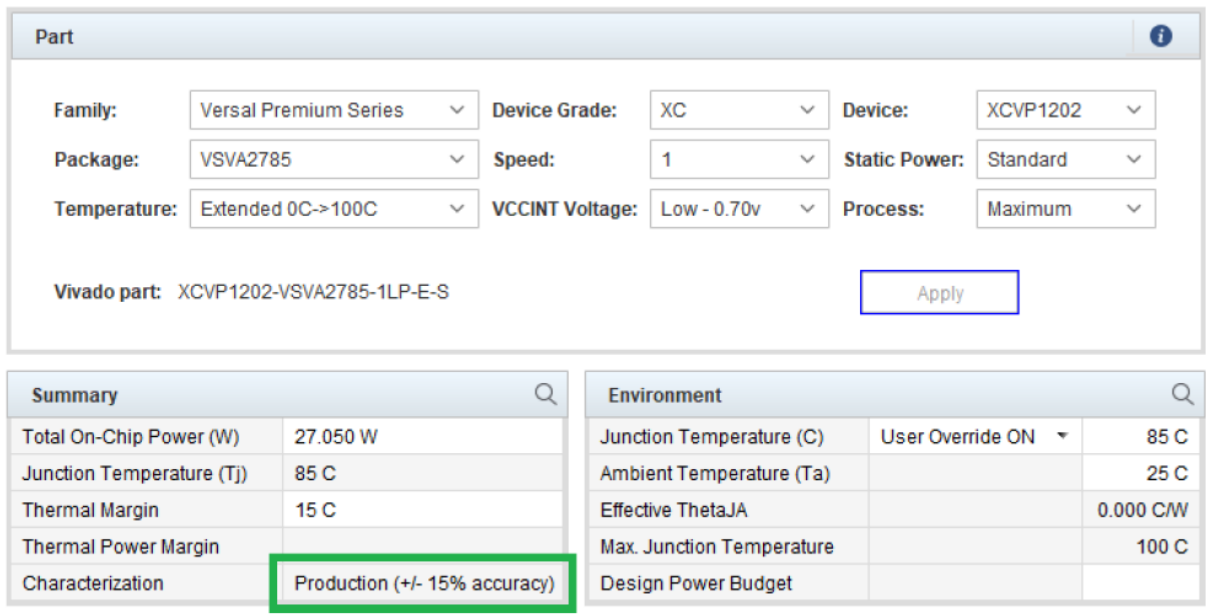
Comparing XPE and PDM power estimates

- XPE & PDM utilise the same power models
- Power correlation expected to be within +-3% when using PRODUCTION models
  - Accounts for rounding, decimal place change between tools
- Wider deviation for devices at PREVIEW, ADVANCE or PRELIMINARY possible
  - These can have minor changes, without causing a change in the Characterisation step
- Devices that change Characterisation between XPE and PDM will also have deviation
  - Example VP1202 will move to PRODUCTION in PDM 2022.2

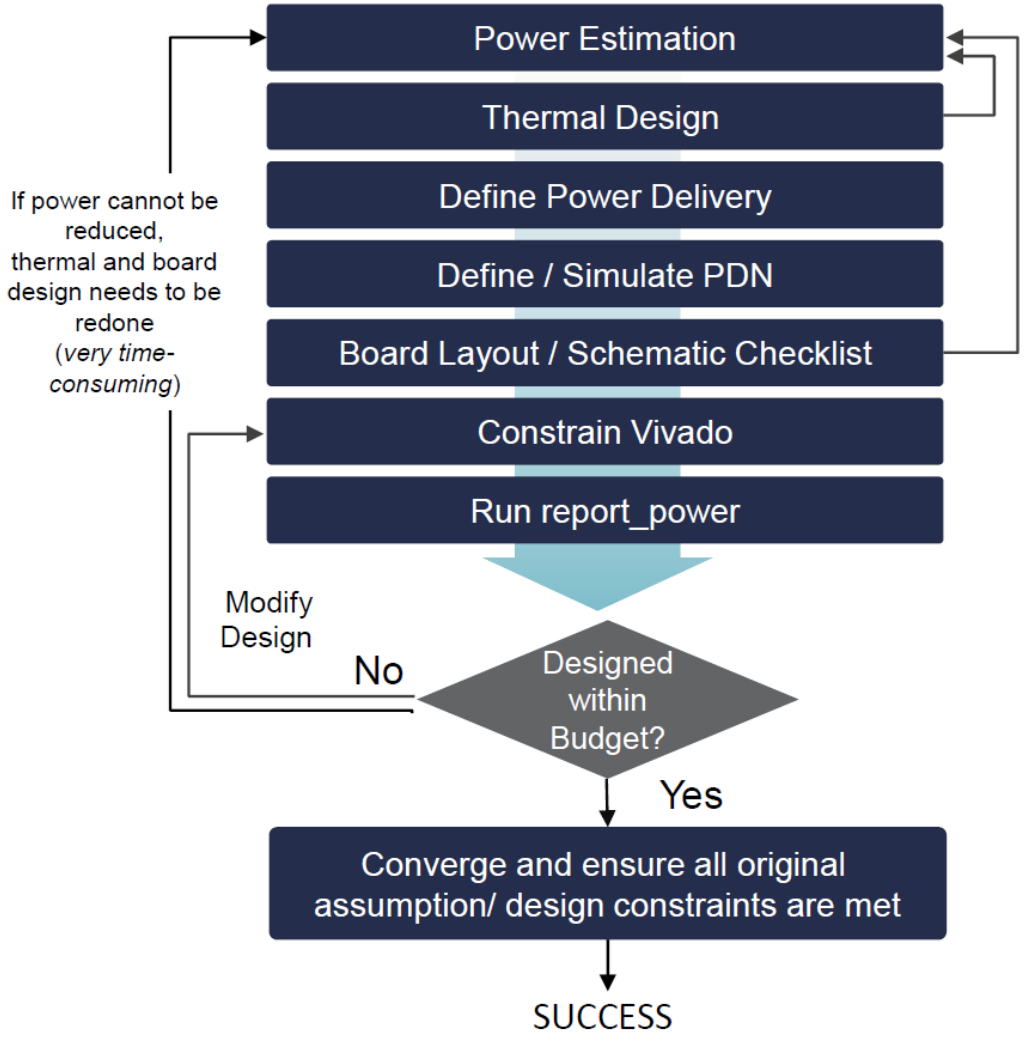


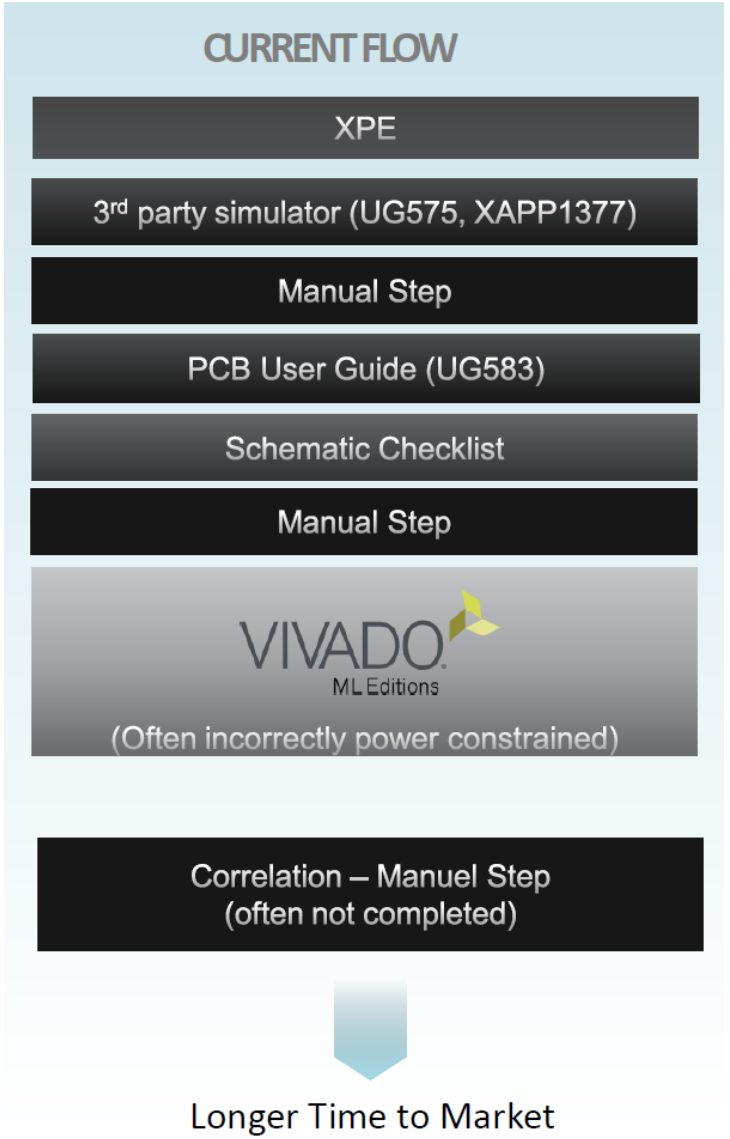


PDM Roadmap

Power Design Manager (PDM)

One Tool for Board Design Methodology

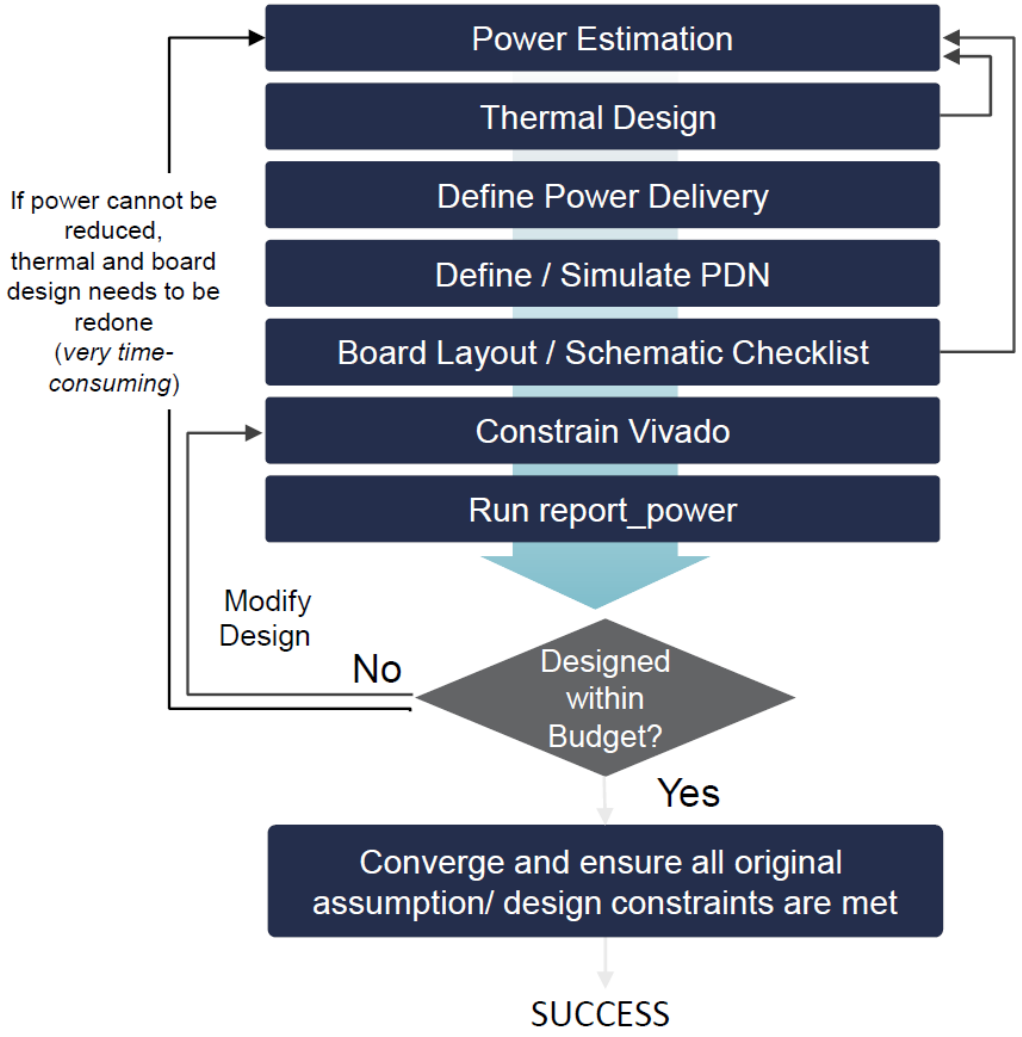


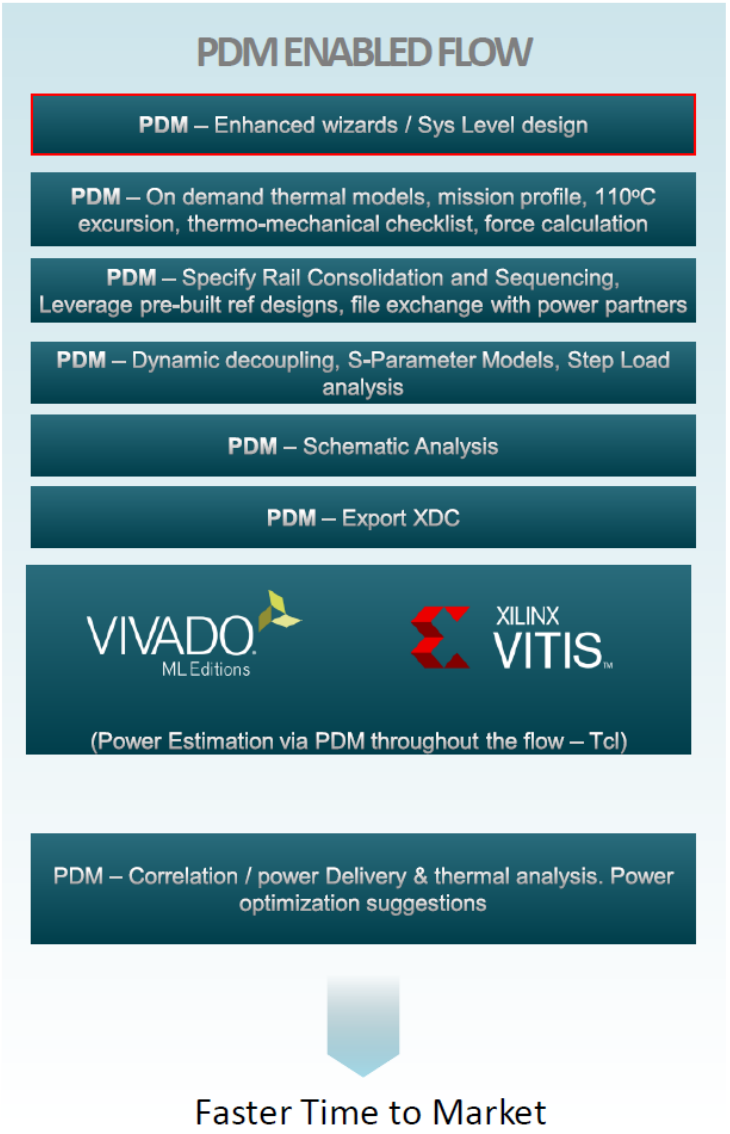


- Fragmented flow
  - Multiple tools and documents
- Prone to error
- Often steps missed
- Incorrect information added
- Problems are costly
  - Longer TTM & TTR

Power Design Manager (PDM)

One Tool for Board Design Methodology





- Cohesive Managed Flow
- Aligned with Methodology
- Integrated approach
  - Addition of other tools
  - Schematic Analysis
  - SEU / FIT tool
  - Power Management
- Goals:
  - Optimal board design
  - Reduce board rework
  - Faster TTM & TTR
  - Improved customer experience
- 2022.2 focus is replacing XPE
  - Additional features 2023/24

Available Resources

- www.xilinx.com/pdm
  - Download standalone PDM install (integration to unified installer planned 2023.1)
  - No Vivado requirement for PDM

- Quick take video for PDM 2022.2 “Introduction to PDM”
  - Covers migration and Wizards
  - Getting Started and Power Design

- Customer training to be updated to PDM –ETA end Nov

- Known issues Answer Record

- Power Design Manager User Guide – UG1556

PDM Demo

Power Design Manager 2022.2 Takeaways

Increased Estimation Accuracy & Integration	• Enhanced Wizards for DDRMC | MRMAC | DCMAC | ILKN | HSC | CPM5 • Generation of XDC constraints • Access to the latest Char models
Easy Migration from XPE	• Fast and effective migration flow from XPE for Versal® portfolio • Re-use existing estimation • Start new estimates for Versal® portfolio using PDM to leverage new features • Import flow from Report Power supported
2022.2 Device and OS Support	• Windows & Linux support • Versal® portfolio: AI Core | AI Edge | Prime | Premium • Kria™: K26 SOM | KV260 Vision AI Starter Kit • For more details visit www.xilinx.com/pdm

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Thank you!

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